



## THE SEMICUSTOM DEVELOPMENT SYSTEM

**DESIGN, VERIFY, AND PROTOTYPE A COMPLETE GATE ARRAY WITH ONE PC-BASED WORKSTATION.**

**FUTURENET MAKES THE POWER OF SEMICUSTOM DEVICES A REALITY.** The latest semicustom technologies give you a new world of opportunity. With these devices, your ability to turn design innovations into profits has never been better. And the performance they provide can meet your highest expectations.

FutureNet®, a worldwide leader of CAE software, now offers you the Semicustom Development System™, a complete gate array workstation that gives you all the power you need to transform your designs into tomorrow's most sophisticated products.

This workstation allows you to quickly and easily design, verify, and prototype a gate array before you go to the manufacturer. And because it supports a wide range of semicustom device technologies, you can easily move from one technology to another.

### **MAINFRAME PERFORMANCE AT A PRICE YOU CAN AFFORD.**

The Semicustom Development System rivals the speed and performance of a mainframe. Yet, it costs substantially less and at the same time, gives you new design capabilities. Built on the open IBM® PC AT architecture, it includes a 32-bit co-processor. This opens up an affordable pathway to powerful simulation and analysis capabilities. And unlike any mainframe system, the Semicustom Development System extends your design power by letting you describe designs functionally, as well as graphically.

### **FUTURENET MAKES GATE ARRAY DESIGN EASY.**

The Semicustom Development System is so easy to learn and use that you'll be able to master it within a few hours. For example, you choose how you want to enter your design, graphically or functionally. You can create your circuit in the way that's most natural to you and most appropriate for the design.

You'll always have help at your fingertips. Extended help displays give you instant access to an on-line user manual. Jump back to the main menu with all your questions answered. Its menu-oriented operation means you won't have to memorize commands.

Now, let's take a closer look at how FutureNet simplifies the design flow.

**FutureNet**  
A Data I/O Company

## GATE ARRAY DESIGN IN THREE EASY STEPS.

### STEP 1: CAPTURE YOUR DESIGNS FUNCTIONALLY, GRAPHICALLY, OR BOTH.

Some aspects of a gate array design are much easier to describe graphically, and others, functionally. Now, for the first time, you have a choice.

The Semicustom Development System lets you quickly draw a schematic of your circuit using DASH™ Schematic Designer. The appropriate foundry symbol libraries are included in the system's design kits. Or for those parts of your design that are better described functionally, use high-level logic expressions. For example, you can describe a sequencer with just a handful of logic equations. Functional description is independent of the target device technology, thus letting you choose your device later in the design process.

The system automatically generates schematics of the parts of your design you've described functionally. These are combined with your DASH schematics to create a complete schematic of your entire design.

### STEP 2: POWERFUL DESIGN VERIFICATION AND SIMULATION ENCOURAGE EXPERIMENTATION.

Verify whether or not your design works the way you intend and improve your circuit — before you go to the gate array manufacturer. The workstation's interactive functional design verifier lets you quickly modify and verify your design. In minutes, you can expand an instruction decoder or change an entire state machine. You'll know immediately whether or not the circuit functions correctly.

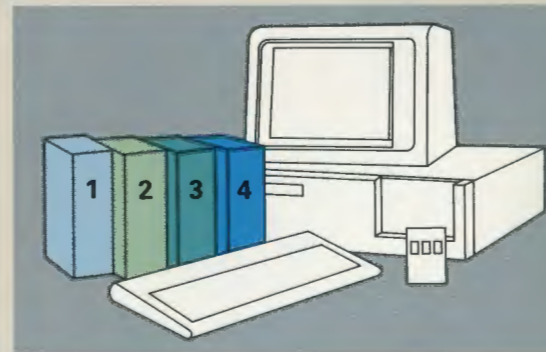
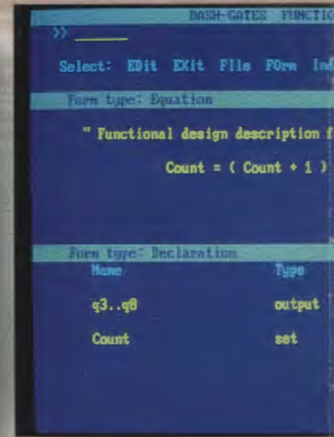
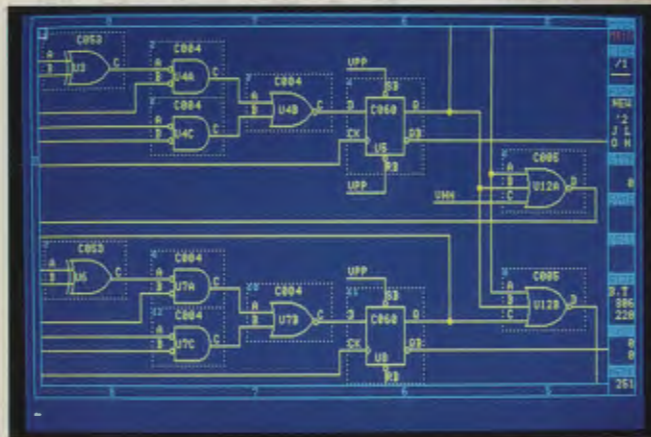
The Semicustom Development System's automatic high-speed logic synthesis algorithm minimizes the number of gates by eliminating any redundancies. Select your final device, and your design

### 1. DESIGN ENTRY

- Draw schematics using DASH Schematic Designer and Semicustom Design Kits containing manufacturer-approved symbol libraries.
- Describe appropriate section functionally using DASH-GATES.
- DASH-GATES automatically generates schematics of the functionally described portions of your design. These are combined with the DASH schematics to create one complete gate array design.

### 2. DESIGN VERIFICATION

- Verify functional description against the DASH schematic.
- Logic simulation automatically generates a fault simulator.
- DASH-GATES forms a complete functional description for simulation.
- Fault simulation forms a complete program.



- 1 Dash Schematic Designer
- 2 DASH-GATES Functional Designer
- 3 DASH-CADAT Plus Logic Simulation,
- 4 Semicustom Design Kits.

## 1. DESIGN ENTRY

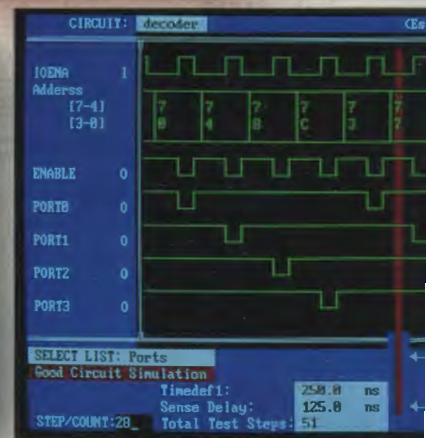
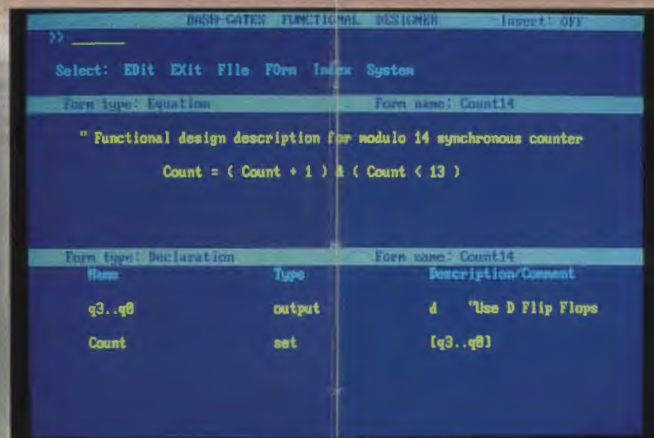
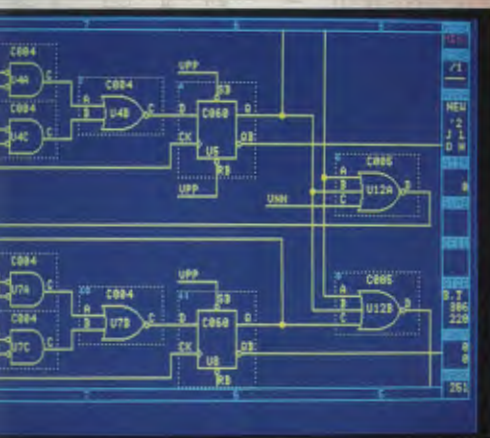
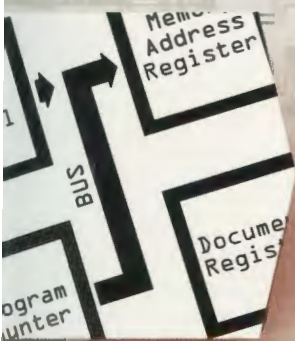
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## 2. DESIGN VERIFY

- Verify (and modify) your functional design using the DASH-GATES interactive design verifier.
- Logic synthesis algorithm automatically reduces and factors the design.
- DASH-CADAT Plus performs simulation and performance analysis using manufacturer-approved simulation models.
- Fault simulation is performed to analyze the test program.

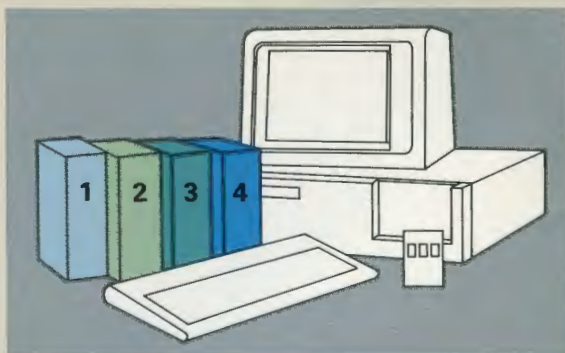
## 3. DESIGN PROTOTYPING

- Partition the design.
- The system automatically produces JEDEC-standard programmer data files.
- Prototype with standard parts and PLDs.
- Documentation is produced.
- Design kits translate the net list to the manufacturer's format.



## FULL DESIGN VERIFICATION ENCOURAGED

Verify whether or not this is the way you intend to build your circuit — before you pay manufacturer. The interactive functional design lets you quickly modify and simulate. In minutes, you can change a decoder or change a machine. You'll know whether or not the circuit will work. The Semicustom Development System's high-speed logic synthesis minimizes the number of iterations, eliminating any redundancies. You'll know whether or not the device, and your design



- 1 Dash Schematic Designer
- 2 DASH-GATES Functional Designer
- 3 DASH-CADAT Plus Logic Simulation
- 4 Semicustom Design Kits.

will be factored to optimize the fit to the device. This lets you trade circuit size against speed.

The workstation also gives you full simulation and performance analysis capabilities. You can identify and correct errors before you go to the time and expense of fabricating devices. It simulates the design using highly accurate manufacturer-approved simulation models included in the design kits.

And, finally, with the Semicustom Development System's fault simulation capability and comprehensive fault reporting, you'll be able to develop a thorough test program that ensures complete testability in production.

## STEP 3: PROTOTYPING BEFORE COMMITMENT

Whether you want to reduce the risk or simply eliminate waste, prototyping your design before you commit to the manufacturer is a smart move. You can debug your design before you build a device that will work. The Semicustom Development System's prototyping capabilities, such as program loader (PLDs), simply partition the system product into PLD programmer.

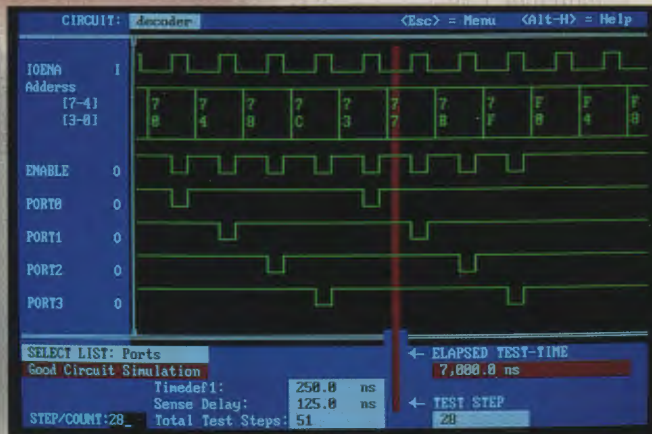
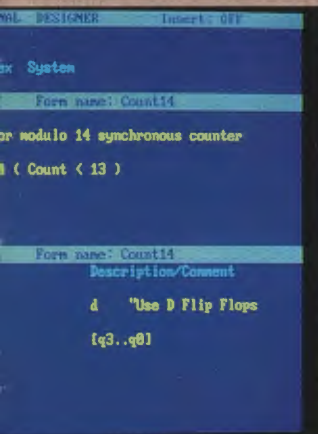
Then, after you've verified your design, you can use a netlist translator to translate your design into a format that the manufacturer's design kits can translate.

## DESIGN VERIFY

and modify your original design using ASH-GATES inter-design verifier. The synthesis algorithm automatically reduces and optimizes the design. I-CADAT Plus performance simulation and performance analysis using manufacturer-approved simulation models. Simulation is performed to analyze the test program.

## 3. DESIGN PROTOTYPING

- Partition the design.
- The system automatically produces JEDEC-standard programmer data files.
- Prototype with standard parts and PLDs.
- Documentation is produced.
- Design kits translate the net list to the manufacturer's format.



The Semicustom Development System allows you to design, verify and prototype a gate array, quickly and easily.

format required by the gate array manufacturer of your choice.

The Semicustom Development System automatically produces documentation of every aspect of design entry, verification, and prototyping. With hard copies of the entire design process, you'll have the added measure of confidence you'll need if you revise your design at a later date. Now, let's look at the workstation programs, one by one.

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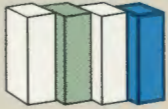
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And, finally, with the Semicustom Development System's fault simulation capability and comprehensive fault reporting, you'll be able to develop a thorough test program that ensures complete testability in production.

**STEP 3: PROTOTYPE YOUR DESIGN BEFORE COMMITTING TO SILICON.** Further reduce the risk of using gate arrays and eliminate weeks of debugging time by prototyping your design before you go to the manufacturer. You can functionally debug your design and confirm that the device will work with the rest of the system. For prototyping with standard parts such as programmable logic devices (PLDs), simply partition your design, and the system produces JEDEC-standard PLD programmer data files automatically.

Then, after you've prototyped and verified your design, use the manufacturer netlist translators included in the design kits to translate your design into the for-

# DASH-GATES: FUNCTIONAL DESCRIPTION TO SCHEMATICS, AUTOMATICALLY.



**YOU'LL NEVER GET LOST IN THE GATES AGAIN.** Because some functions such

as sequencers, decoders, and state machines are awkward to describe gate by gate, the Semicustom Development System gives you DASH-GATES™. This is the only tool that lets you describe even the most complex logic circuits using any combination of truth tables, state diagrams, and logic expressions. You don't have to fit your design style to your system; it adapts itself to you.

With DASH-GATES, you don't need to specify the physical layout of the circuit, just what the circuit will do. You simply describe the outputs as a function of the inputs, not how the circuit should implement the function, how it will look, or how many individual gates it will require. Once you use DASH-GATES, you'll find that designing at the functional level is much like writing software in a high-level language rather than machine code. It's faster, the results are more accurate and reliable, and it's much easier to modify the initial design.

## NO MORE TIME-CONSUMING REVISIONS.

Not only is functional design entry easy, but DASH-GATES makes design revisions just as convenient and fast. The software includes an interactive design verifier which is driven by your original design description. This allows you to specify the stimulus and examine the response with the same signal and state names as used in your design. Therefore you can validate changes instantly without exiting the program.

In fact, the DASH-GATES verifier is an extremely helpful "what if" tool. Other simulators are typically batch processors, upsetting the natural design iteration cycle. The verifier tracks parts of the design you have changed, and only those parts will be reprocessed, saving you even more time. It works much like a spreadsheet: Change a value, and watch the results ripple through your design. You can experiment with many different design ideas until you achieve precisely the results you want, well before you commit to silicon.



DASH-GATES allows designs to be captured functionally using any combination of logic equations, state diagrams, and truth tables.

Form type: Equation	
" Functional design description f	
Count = ( Count + 1 )	
Form type: Declaration	
Name	Type
q3..q8	output
Count	set

Form type: State	
" Functional Design Descriptio	
State: Floor1	
Equations:	
Light1 = True	
Case: Up_select == True	
Goto: Floor2	
Form type: Declaration	
Name	Type
One,Two,Three,Four	input
q3..q8	I/O
Out_state	set
Up_select,On_select	I/O

Form type: Truth-Table				
Digit	A	B	C	D
0	On	On	On	On
1	Off	On	On	Off
2	On	On	Off	On
3	On	On	On	On
4	Off	On	Off	Off
Form type: Declaration				
Name	Type			
A,B,C,D,E,F,G	output			
q3..q8	input			
Digit	set			
On	macro			

**DASH-GATES AUTOMATICALLY SYNTHESIZES YOUR DESIGN.** A high-speed logic synthesis algorithm minimizes the number of gates automatically. You won't have to weed out unnecessary gates, a task that's time consuming, error prone, and sometimes impossible to accomplish by hand.

First, DASH-GATES converts the design to a sum-of-products form by expanding any set notation and macros, and replacing high-level mathematical operators with four standard Boolean operators (AND, NOT, OR, and EXCLUSIVE OR). The program then reduces the logic by eliminating any redundancies to minimize circuit size. DASH-GATES resolves any "don't care" values, setting them to whatever values will result in the lowest gate count.

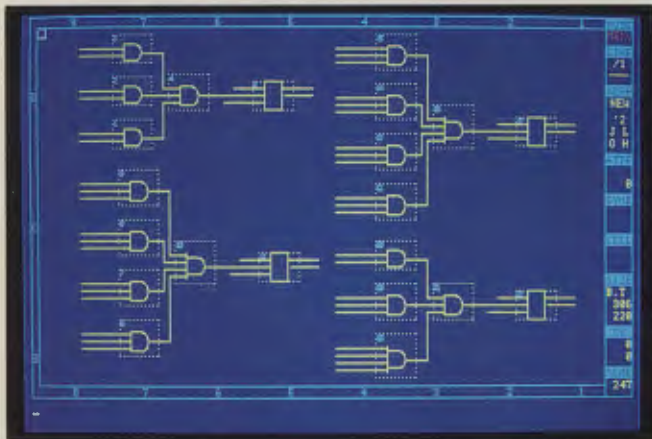
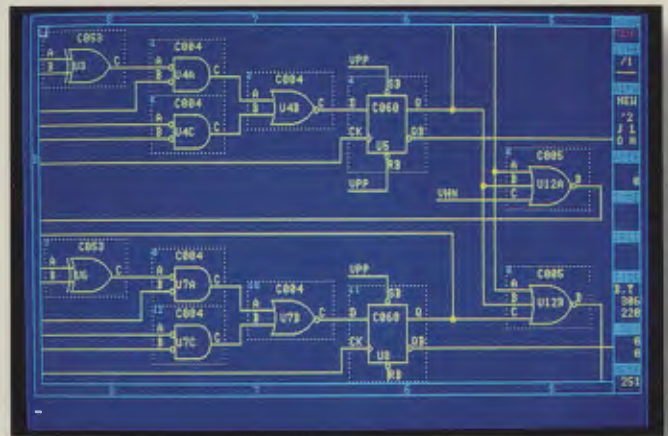
Because you can specify "don't care" information for outputs, the logic reduction algorithm can generate even fewer gates.

The DASH-GATES algorithm then factors your design to optimize the fit to the target device, trading circuit size against speed. Factoring detects and extracts terms which are used several times in a set of equations. To minimize real estate requirements, it generates these terms once and distributes them to multiple outputs, so that the same logic function may be implemented with fewer and smaller gates. When speed is most important, the sum of products implementation may be used.

By eliminating redundant gates, DASH-GATES improves overall circuit testability as well. Testing can only verify



## DASH SCHEMATIC DESIGNER: CREATE SCHEMATICS AT LIGHTNING SPEED.

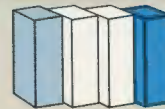


that, for a given input, the output will have the desired value. It's impossible to look inside the device to determine the path that the signal took to reach the output. Therefore, if the circuit has more than one redundant path to the same output, the test results for that output will not be reliable.

Once your functional design is fine-tuned, an automatic schematic generator instantly draws a DASH schematic of it using JEDEC-standard gate array macrocells.

For those portions of the design that were captured functionally, DASH-GATES automatically generates schematics using gate array macrocells.

Use DASH Schematic Designer with semicustom symbol libraries to easily draw those portions of your circuit that are best described graphically.



To complete design entry, the Semicustom Development System gives you

instant access to the powerful features of DASH Schematic Designer, one of the most sophisticated schematic capture packages available.

Use the manufacturer symbol libraries included in the Semicustom Design Kits to easily draw the parts of your circuit which are best described graphically, like data paths. Then combine these schematics with those drawn by DASH-GATES to create a schematic of the entire circuit.

You won't have to create your own parts libraries. Simply call up the parts you need from DASH's extensive libraries, which support TTL, ECL, CMOS, Memory, Discrete, Intel, Motorola, and IEEE parts. Other libraries such as IBM flowchart symbols and Mil D 1000 are also available. When you want the flexibility to add custom libraries, you can easily create your own custom symbols using the DASH symbol editor.

Once you become proficient using DASH, you'll appreciate its incredible speed. Not only does DASH generate

schematics quickly, but it includes several special modes that minimize keystroking. For example, you can bypass menus and help displays, write macros to abbreviate long instructional sequences, and define function keys to do specific tasks. If you're oriented towards using a mouse, there's one at your fingertips.

Advanced users will enjoy the full power of DASH's sophisticated drawing features, like tag and drag. With a click of the mouse, you can target a symbol, drawing area, or alphanumeric field and copy, move, or delete it. As you move connected symbols or areas across the screen, orthogonal rubber banding maintains original connections. New lines are automatically drawn at 90 degree angles.

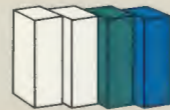
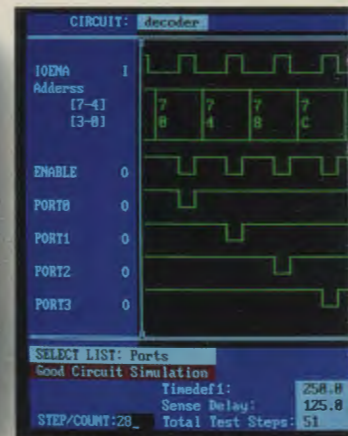
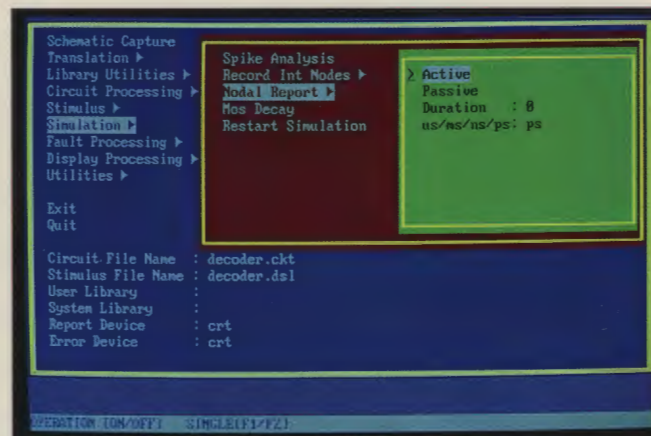
You can also rotate a symbol around its center, and reflect it to create the mirror image. Another DASH feature, layered alpha text, lets you hide up to 4,096 characters under one displayed text field, giving you more flexibility to store data in your drawings.

DASH supports hierarchical type designs, allowing you to create your schematic from top-down, bottom-up, or any point in between. You can also define your design with increasing detail, up to 99 levels deep. When you edit your schematic, changes are automatically incorporated throughout the design. It's this hierarchical structure that allows you to bury the schematic generated by DASH-GATES within the DASH schematic.

### DESIGN KITS HELP YOU PREPARE FOR THE MANUFACTURER, EVERY STEP OF THE WAY.

Semicustom Design Kits, included with the Semicustom Development System, give your workstation the necessary gate array manufacturer-specific information for developing semicustom devices. The kits include the Symbol Libraries needed to create a schematic of your semicustom device in DASH, a Netlist Translator which formats a compatible netlist for the manufacturer of your choice and Simulation Libraries, so you can use DASH-CADAT Plus to simulate not only the specific gate array, but the complete design. You'll go to the manufacturer confident that your device works by itself and within the rest of the circuit.

## DASH-CADAT PLUS: LOGIC SIMULATION IDENTIFIES ERRORS BEFORE PROTOTYPING.



Debug your design using DASH-CADAT Plus as a software breadboard.

The Simulation Libraries offer highly accurate modeling of gate array macro-cells. They also add two major levels of semicustom simulation to DASH-CADAT Plus, one of the most powerful simulators on the market.

First, functional simulation gives you a quick check whether the logic is correct and a rough estimate of timing. Use this for fast turnaround.

Second, when you're ready to run a complete simulation, performance analysis gives you comprehensive and precise information. It provides detailed timing information including pin-to-pin delays, setup/hold, minimum pulse widths, race, hazard and spike conditions. You can study device layout effects, and fanout loading to determine the timing effects of loading and layout.

### THE POWER OF A MAINFRAME SIMULATOR.

DASH-CADAT Plus has much greater capacity and speed than other desktop simulators. The workstation includes a 32-bit co-processor board and a 4 MB of memory, so it can handle designs that have 30,000 gates or more. Menu-oriented operation and on-line help make all this power easy to use.

### FAMILIAR LOGIC ANALYZER GRAPHICS FOR EASIER CIRCUIT ANALYSIS.

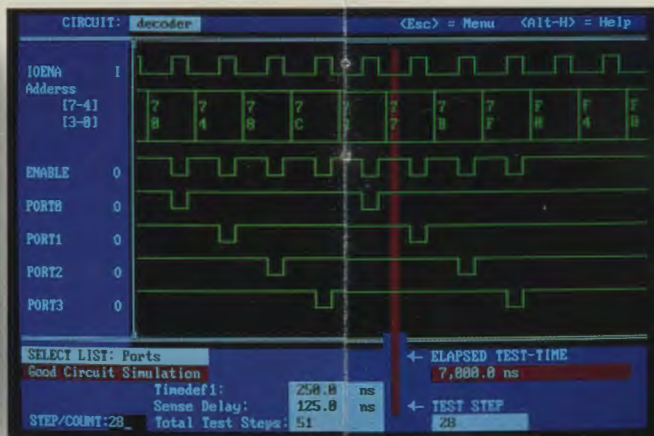
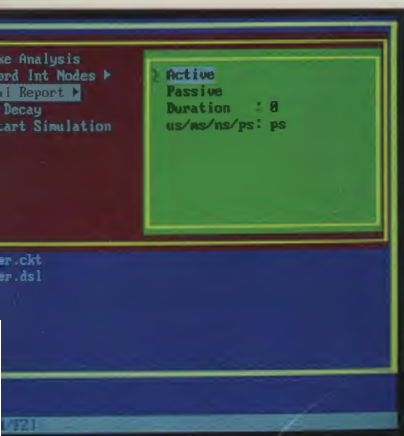
The display of simulation waveforms looks just like a logic analyzer. Working with familiar graphics makes circuit and timing analysis second nature. View simulated activity on any node in the circuit, at any point in time, down to 100 picoseconds. You'll be able to catch and correct problems that are impossible to track down with a real breadboard and logic analyzer.

### FAULT SIMULATION BUILDS TESTABILITY INTO YOUR PRODUCTION MODEL.

Using the same circuit and stimulus files, DASH-CADAT Plus automatically generates files containing all the information needed for fault simulation. The program's concurrent, functional technique makes it one of the fastest fault simulators available today. And it works equally well no matter how the circuit is modeled, whether it's at the transistor, gate, functional, or behavioral level.

And for writing test vectors, our high-level language gives you enough versatility to define simple or complex stimulus, quickly and painlessly. You can, for example, define a set of frequently used stimulus as a macro and recall it with a single command. Then pass arguments to the macro as the stimulus is expanded, and save yourself hours of work. With the vectors function, you can treat a group of

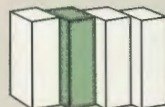
# PLUS: LOGIC IDENTIFIES PROBLEMS



LEFT: Menu-oriented operation makes the power of DASH-CADAT Plus extremely easy to use.

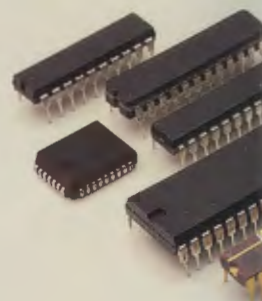
RIGHT: The waveform display looks just like a logic analyzer, making circuit analysis simple. Select any signal, at any point in time, down to 100 picoseconds.

## PLD PROTOTYPING YOU TRY OUT CIRCUIT.



PLDs. Simply specify what you want in each segment and the program will automatically calculate the resources required and produce a PLD programmer load file.

PLD prototyping hardware gate array works with customer feedback to produce silicon to be sure the product meets their needs. And DASH-CADAT Plus is extremely easy to modify a PLD array without making a new design.



Debug your design using DASH-CADAT Plus as a software breadboard. It offers highly detailed timing information on any node in the circuit, at any point in time, down to 100 picoseconds. You'll be able to catch and correct problems that are impossible to track down with a real breadboard and logic analyzer.

Simulation gives you a clear view of the logic is correct or not. Use this

simulation ready to run a performance analysis. DASH-CADAT Plus offers precise timing information, such as pin-to-pin delays, pulse widths, race conditions. You can analyze fanout and fanout timing effects.

### FRAME SIMU-

DASH-CADAT Plus has much more speed than other simulators. The workstation processor board and software it can handle 100 gates or more. On-line help is easy to use.

**FAMILIAR LOGIC ANALYZER GRAPHICS FOR EASIER CIRCUIT ANALYSIS.** The display of simulation waveforms looks just like a logic analyzer. Working with familiar graphics makes circuit and timing analysis second nature. View simulated activity on any node in the circuit, at any point in time, down to 100 picoseconds. You'll be able to catch and correct problems that are impossible to track down with a real breadboard and logic analyzer.

**FAULT SIMULATION BUILDS TESTABILITY INTO YOUR PRODUCTION MODEL.** Using the same circuit and stimulus files, DASH-CADAT Plus automatically generates files containing all the information needed for fault simulation. The program's concurrent, functional technique makes it one of the fastest fault simulators available today. And it works equally well no matter how the circuit is modeled, whether it's at the transistor, gate, functional, or behavioral level.

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pins as a single pin and handle all lines of a data bus as a single unit. Or use the waveform specification capability to specify clocking sequences and asynchronous waveforms.

**TRACK DOWN UNDETECTED FAULTS FASTER.** The program generates a comprehensive set of fault reports that help you quickly track down faults your test program doesn't cover. The statistical fault trace list, for example, shows the chain reaction of events caused by each fault. Use it to find hot spots, where the density of fault effects is high. You'll finish with the highest possible confidence in your design implementation.





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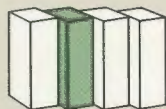
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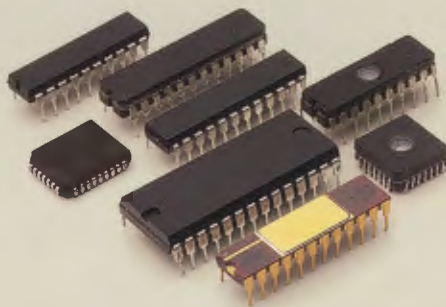
## PLD PROTOTYPING LETS YOU TRY OUT YOUR CIRCUIT.



DASH-GATES allows you to easily partition your design for prototyping with

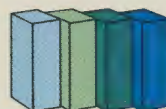
PLDs. Simply specify which outputs you want in each segment. DASH-GATES will automatically calculate the inputs required and produce JEDEC-standard PLD programmer load files.

PLD prototyping helps verify that your gate array works with the rest of the system you've designed. You can also get customer feedback before committing to silicon to be sure the product meets all of their needs. And DASH-GATES makes it extremely easy to move from PLD to gate array without making any changes in the design.



Functional capture, using DASH-GATES, is technology independent. Simply partition your design and programmable logic data files are formed automatically.

## AUTOMATIC DOCUMENTATION SAVES YOU VALUABLE DESIGN TIME.

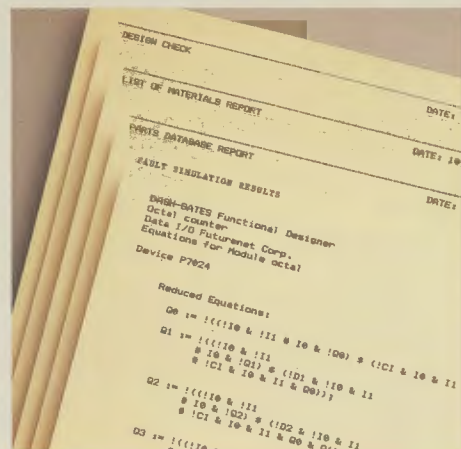


The Semicustom Development System automatically produces hard copies of

every aspect of the design process. For example, List of Materials provides a printout of the parts used in your design, giving production engineers an easy way to determine costs and inventory requirements. Design Check identifies errors, such as nets with no connections or only one connection, unconnected pins, duplicate circuit designators, and illegal logic nets.

For documenting the simulation process, DASH-CADAT Plus provides comprehensive fault reports. It identifies and traces all failure modes, helping you work towards full testability.

With hard copies of every step, you'll be able to easily reconstruct your design whenever you need to make revisions.



Documentation is generated automatically for each stage of the design process.

## COMPREHENSIVE CUSTOMER SUPPORT SERVICES.

With FutureNet's complete range of after-the-sale services, you'll have the support you need. In fact, our Customer Support Services begin even before your system is installed, with a free training seminar.

A standard warranty is included with every workstation you buy. You may also purchase a Software Update Service and Hardware Support Agreement which includes product updates automatically. And you can call our Technical Assistance group for free applications assistance at any time.

As a FutureNet customer, you're also eligible to join the FutureNet Users Network (FUN) for a nominal fee. (Membership is included with all support agreements.) This valuable Network group gives you a way to share new application discoveries with your colleagues. And on a quarterly basis, you'll receive a newsletter full of helpful information plus a listing of utility programs written by other members, and available to you.

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